

A 44 GHz HEMT Doubler/Amplifier Chain

P.D. Chow, Y. Hwang, D. Garske, J. Velebir, and H. C. Yen

TRW Electronic Systems Group
One Space Park
Redondo Beach, CA 90278

Abstract

A 44 GHz doubler was designed and fabricated using 100x 0.15 μm InGaAs HEMT and MIC circuit. The doubler shows a minimum conversion loss of 1.4 dB with 0.4 dBm output power, and 1.6 dBm maximum output power with 3.4 dB conversion loss. A 44 GHz InGaAs HEMT doubler/amplifier chain was also fabricated, demonstrating 10 dBm power, 7 dB overall gain, and 2 GHz bandwidth at the output frequency.

Introduction

GaAs MESFETs have been used extensively for frequency doubling at microwave and millimeter (mm) wave frequencies [1-7]. Good output power has been reported on these MESFET doublers. Due to its superior material properties, the InGaAs HEMT has demonstrated better power-added efficiency and output power than a MESFET or GaAs HEMT with comparable size at mm wave frequency. The possibility of using InGaAs HEMT for high frequency doubler application has not been explored. This paper describes the computed and measured performance of a low conversion loss 44 GHz doubler using InGaAs HEMT device and MIC circuit. To our knowledge, this is the first reported 44 GHz HEMT doubler. To demonstrate the feasibility of using this doubler as the LO source or frequency translator in future Q-band satellite communication systems, we will also show the performance of a wideband doubler/amplifier chain fabricated using the doubler and a Q-band three-stage InGaAs HEMT amplifier. A HEMT-based doubler/amplifier chain is amenable to monolithic implementation for further size reduction and integration with other components (e.g., HEMT LNA/mixer).

Device Selection and Circuit Design

Pseudomorphic Indium Gallium Arsenide (InGaAs) HEMTs with 0.15 μm gate length and 80 or 100 μm gate widths were employed in both the doubler and the three-stage

amplifier fabrication. The AlGaAs/InGaAs heterostructure of our device was grown by MBE and the 0.15 μm gate was patterned by electron beam lithography. To achieve higher breakdown voltage for higher power handling capabilities, the AlGaAs region was undoped except in a thin layer near the AlGaAs/InGaAs interface which is doped heavily with Si.

Figure 1 shows the circuit configuration of the 22/44 GHz HEMT doubler. The doubler input port was matched to receive maximum power at the fundamental frequency 22 GHz.

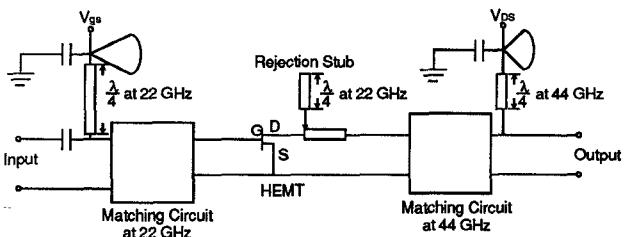


Figure 1. Circuit Configuration Of The 44 GHz HEMT Doubler

The output was matched to deliver maximum power at second harmonic frequency 44 GHz. Quarter-wavelength stub was used to reject the second harmonic frequencies at drain. To gain some insight into the doubler operation, we have constructed a nonlinear model for our InGaAs HEMT devices using the Curtice-Ettenberg model [8]. The modelling parameters were derived from the device small signal equivalent circuit and measured DC characteristics. The small signal equivalent circuit was in turn derived from measured 2-26 GHz S-parameters. The doubler performance was calculated using this HEMT nonlinear model in conjunction with a nonlinear circuit analysis program (EESOF LIBRA). Figure 2 shows the calculated second harmonic output power vs. gate bias at 22 GHz fundamental frequency and 4 dBm input power. As expected, it indicates that the HEMT device should be biased near pinch-off to generate the most second

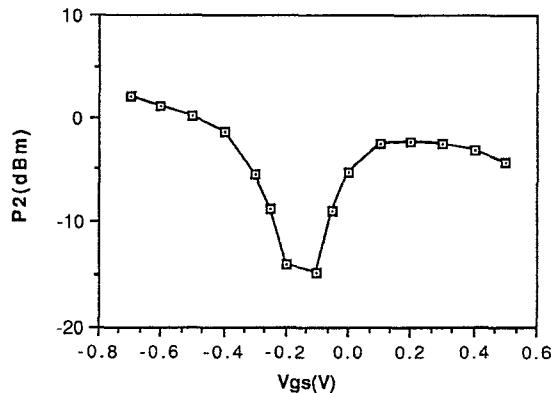


Figure 2 Calculated second harmonic output power vs. gate bias of $100 \times 0.15 \mu\text{m}$ InGaAs HEMT at 22 GHz fundamental frequency. Input power = 4 dBm.

harmonic power. Figure 3 illustrates the calculated drain current waveform for one cycle at 22 GHz fundamental frequency of a HEMT doubler biased near pinchoff. Second harmonic content in the drain current waveform becomes much more significant at 4 dBm input power than at -10 dBm drive. The calculated output power of the doubler is compared with the measured data below.

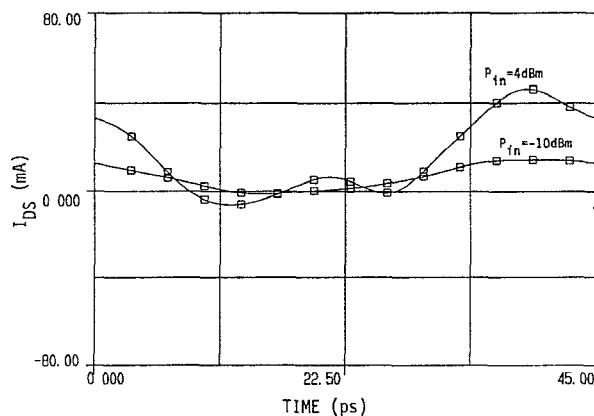


Figure 3 Calculated drain current waveform for one cycle at 22 GHz fundamental frequency of a $100 \times 0.15 \mu\text{m}$ InGaAs HEMT biased near pinchoff.

Experimental Results

Doubler

The doubler circuit was fabricated on 10 mil quartz substrate using $100 \times 0.15 \mu\text{m}$ InGaAs HEMT. A K-connector and a finline waveguide-to-microstrip transition were used at the input and output ports, respectively. Figure 4 shows the measured conversion loss and 44 GHz output power as a function of input power at 22 GHz. The dou-

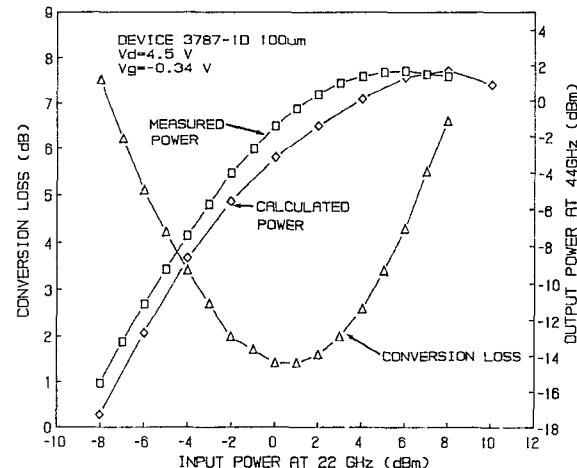


Figure 4 Measured conversion loss and 44 GHz output power of the doubler as a function of input power at 22 GHz. The measured and calculated 44 GHz power output are also compared.

bler shows a minimum conversion loss of 1.4 dB with 0.4 dBm output power and 1.6 dBm maximum output power with 3.4 dB conversion loss. The DC drain current and hence the total dc power consumption vary with the input power, but in no case the DC power is over 50 mW. Figure 4 also compares the measured and calculated 44 GHz power output as a function of input RF power. The calculated power is lower than the measurement by 0.5 to 1 dBm. A good agreement is achieved in the saturated output power. To achieve a good agreement, we found that it is essential to include the higher order (3rd to 6th) harmonics and the bias dependence of pinchoff voltage in the simulation. Figure 5 shows the output power vs. output frequency. It has 2 GHz bandwidth centered at 44.5 GHz for output power higher than 0.5 dBm.

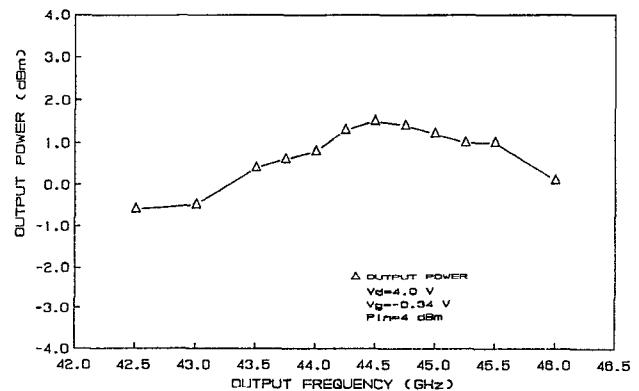


Figure 5 The output power vs. output frequency of the doubler. Input power = 4 dBm.

Three-Stage InGaAs HEMT Amplifier

A MIC three stage amplifier was designed and fabricated using $80 \times 0.15 \mu\text{m}$ InGaAs HEMT devices to amplify the output of the doubler to 10 dBm level. Figure 6 shows a photo of this amplifier. Figure 7 shows the measured gain and input return loss from 43 to 46 GHz at -20, -5, and 0 dBm input power. The linear gain is 16 dB. Total DC power consumption is less than 170 mW for all three stages. The 1-dB compression input and the saturated output power is -10 dBm and 10 dBm, respectively. All these data include about 1 dB waveguide-to-microstrip finline transition loss.

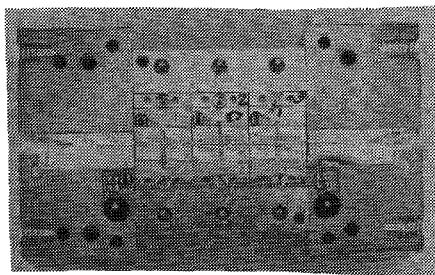


Figure 6 Photo of the three-stage InGaAs HEMT MIC amplifier.

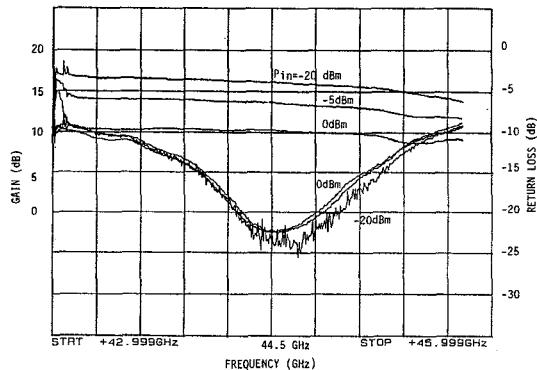


Figure 7 Measured amplifier gain and input return loss from 43 to 46 GHz at -20, -5, and 0 dBm input power.

Doubler/Amplifier Chain

A 44 GHz microstrip bandpass filter was used following the doubler to prevent saturation and spurious signal generation in the amplifier. This three section, edge-coupled bandpass filter was fabricated on 10 mil quartz substrate and showed less than 3 dB insertion loss with 4 GHz bandwidth. It has better than 40 dB rejection at 22 GHz. Figure 8 is a photo of the assembled 44 GHz doubler and the microstrip bandpass filter.

The doubler/filter assembly and the three-stage amplifier were cascaded

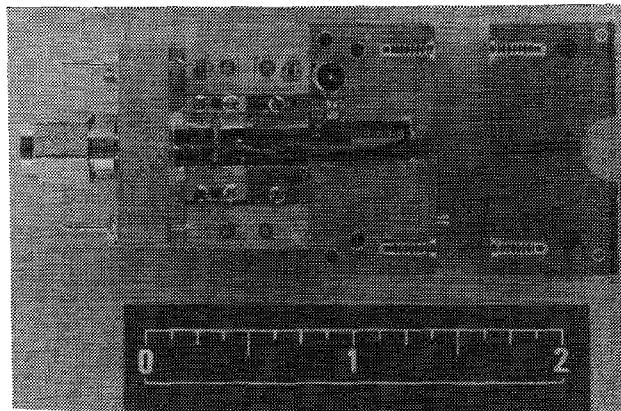


Figure 8 Photo of the assembled 44 GHz doubler and the microstrip bandpass filter.

together and tested without further tuning. Figure 9 shows the measured output power and gain of this doubler/amplifier chain.

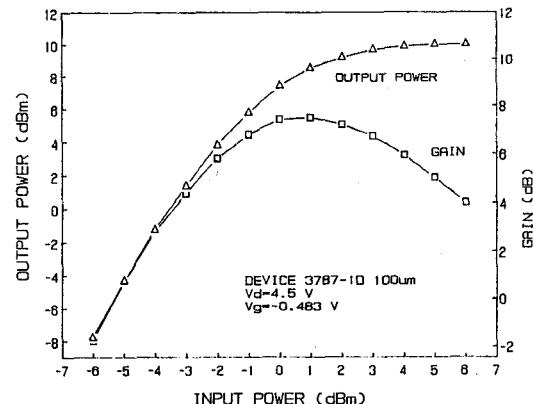


Figure 9 Measured output power and gain of the 44 GHz doubler/amplifier chain as a function of input power at 22 GHz.

It is capable of delivering 10 dBm power at 44 GHz with 6 dB associated gain. The maximum gain is 7.5 dB with 8.5 dBm output power. These results include the 0.25 dB connector loss and 0.5 dB waveguide-to-microstrip transition loss. The measured output power as function of the output frequency is shown in Figure 10. It has 2 GHz bandwidth for output power over 10 dBm.

Conclusion

A low conversion loss 44 GHz MIC doubler was designed and fabricated using $100 \times 0.15 \mu\text{m}$ InGaAs HEMT device. The doubler shows a minimum conversion loss of 1.4 dB with 0.4 dBm output power and 1.6 dBm maximum output power with 3.4 dB conversion loss. The doubler large signal performance was calculated using harmonic balance technique and a nonlinear HEMT model. The calculated and measured results showed reasonable agree-

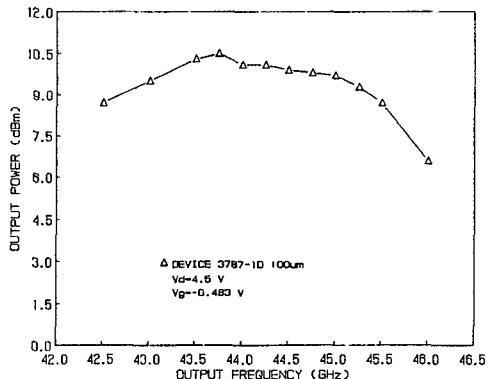


Figure 10 Measured output power as a function of output frequency of the 44 GHz doubler/amplifier chain. Input power = 4 dBm.

ment. A doubler/amplifier chain was also fabricated, demonstrating 10 dBm output power, 7 dB overall 22/44 GHz power gain, and 2 GHz bandwidth at the output frequency. The results presented in this paper demonstrate the feasibility of a HEMT-based doubler/amplifier chain for use as the LO source or frequency translator in future Q-band satellite communication systems.

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REFERENCES

1. A. Gopinath, and J. Rankin, "Single-gate MESFET Frequency Doubler," IEEE Trans. Microwave Theory Tech., vol. MTT-30, pp 869-875, June 1982.
2. M. Gupta, R. Laton and T. Lee, "Performance and Design of Microwave FET Harmonic Generators," IEEE Trans. Microwave Theory Tech., vol. MTT-29, pp. 261-263, March 1981.
3. C. Rauscher, "High-frequency Doubler Operation of GaAs Field-Effect Transistors," IEEE Trans. Microwave Theory Tech., vol. MTT-31, pp. 462-473, June 1983.
4. T. Saito, et al., "A 45 GHz GaAs FET MIC Oscillator-Doubler," IEEE MTT-S Digest, pp 283-285, 1983.
5. S. Meszaros et al., "An integrated 18.75/37.5 GHz FET frequency doubler," IEEE MTT-S Digest, pp. 815-818, 1988.
6. J. Geddes, V. Sokolov, and A. Contolatis, "W-band GaAs MESFET Frequency Doubler," IEEE Microwave and Millimeter Wave Monolithic Circuit Symposium Digest, pp. 7-10, 1987.
7. K. Ogawa et al., "A 50 GHz GaAs FET MIC Transmitter/Receiver Using Hermetic Miniature Probe Transitions," IEEE Trans. Microwave Theory Tech., Vol. MTT-37, pp. 1434-1441, Sept. 1989.
8. W.R Curtice and M. Ettenberg, "A Nonlinear GaAs FET Model for Use In the Design of Output Circuit for Power Amplifiers," IEEE Trans. Microwave Theory Tech., vol. MTT-33, pp. 1383-1393, 1985.